



VeGen

A Vectorizer Generator for SIMD and Beyond

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low we target non-SIMD vector instructions today

[X86] Improve the selection of SSE3/AVX addsub instructions.

[x86] Remove the last vestiges of the BLENDI-based ADDSUB pattern matching.

[X86] Merge ADDSUB/SUBADD0 detection into single methods that can detect either...

[X86] Add ISEL patterns to select SSE3/AVX ADDSUB instructions.

[X86] Merge ADDSUB

Description

Previously, we called

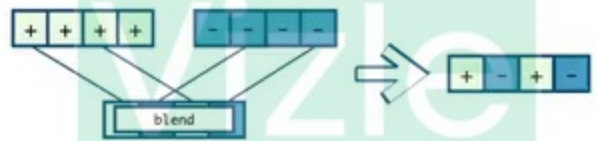
Differential Revision:

Sum-ids: 327730

Description

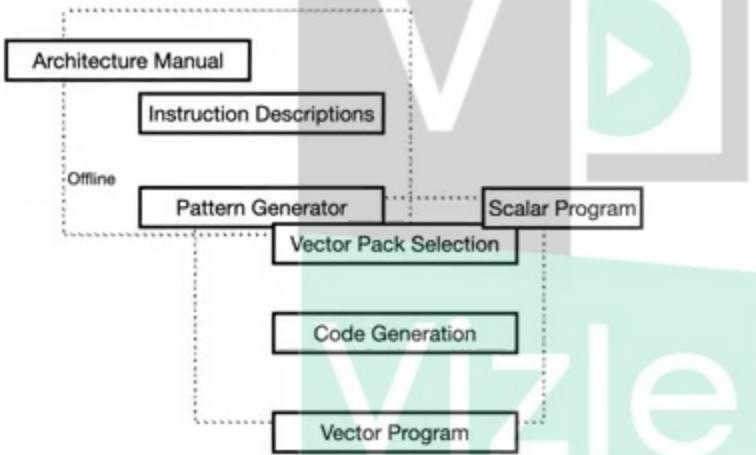
[X86] Add ISEL patterns to select SSE3/AVX ADDSUB instructions.

This patch adds ISEL patterns to select SSE3/AVX ADDSUB instructions from a sequence of 'vadd + vsub + blend'.





veGen: Our Vectorizer Generator for extracting *Lane Level Parallelism*

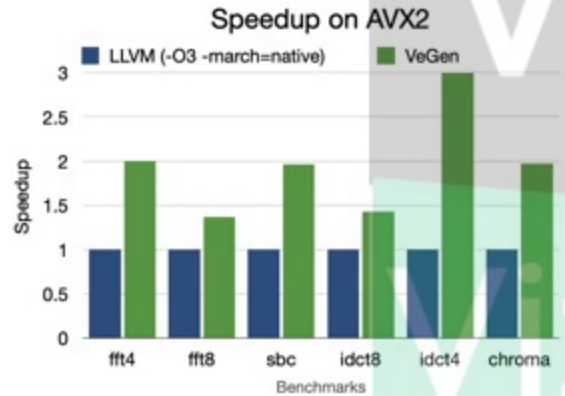


Bottom-up Vector Pack Selection





Benchmarking DSP kernels from FFmpeg and x265





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