



Zedboard Video Interface with VGA

Vipin Kizheppatt

Vizle



<https://vizle.offnote.co>

Contact us: vizle@offnote.co

This document was generated automatically by **Vizle**

Your **Personal Video Reader Assistant**

Learn from Videos **Faster** and **Smarter**

VIZLE PRO / BIZ

- Convert *entire* videos ^{PDF, PPT}
- *Customize* to retain all essential content
- Include Spoken *Transcripts*
- Customer support

Visit <https://vizle.offnote.co/pricing> to learn more

VIZLE FREE PLAN

- Convert videos *partially* ^{PDF only}
- Slides may be *skipped**
- Usage restrictions
- No Customer support

Visit <https://vizle.offnote.co> to try free

Login to Vizle to unlock more slides*

Frame Rate

- Number of frames/second
- Most of our displays run at 50Hz or 60Hz frame rate → 50 frames/second or 60 frames/second
- So for at 1080p resolution, 60Hz frame rate with 1 byte for each color component (RGB), the required raw throughput will be

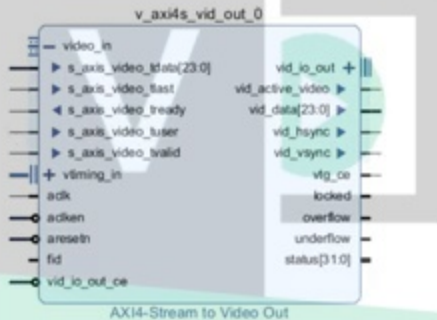
$$1920 \times 1080 \times 60 \times 3 = 373.248 \text{ MB/s}$$

Vizle

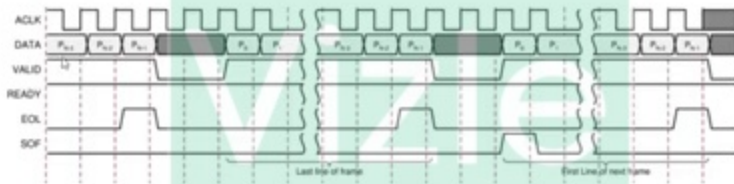
Pixel Clock

- You can see there are very strict time requirements regarding the duration of different signals
- So these signals must be synchronized with a clock with very specific frequency, called **pixel clock**
- For VGA, one pixel will be transmitted/pixel clock
- But the clock signal is not transmitted to the display
 - There are historic reasons for it
 - VGA is an analog standard initially developed for CRT displays but current digital displays also support them as a legacy interface

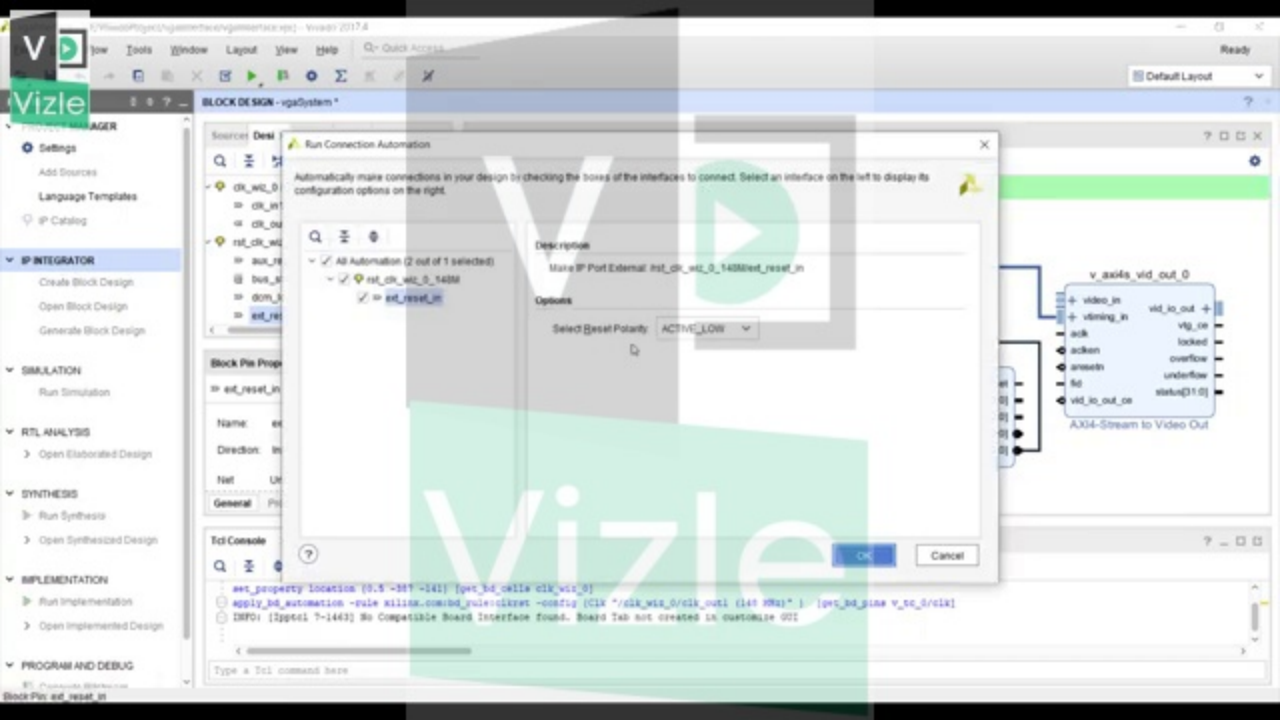
Xilinx AXI4-Stream Video Out



AXI4-Stream to Video Out



Timing diagram



Run Connection Automation

Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.

- All Automation (2 out of 1 selected)
 - rst_dr_wiz_0_140M
 - rst_reset_in

Description

Make IP Port External: rst_dr_wiz_0_140M/reset_in

Options

Selected Reset Polarity: ACTIVE_LOW

OK

Cancel

Block Pin Properties

Block Pin Properties for: rst_reset_in

Name: rst_reset_in

Direction: Input

Net: UNRESOLVED

General Properties

Tcl Console

```
set_property location {0.0-301-141} [get_bd_cells clk_wiz_0]
apply_bd_automation -rule xilinx.com:bd_rule:clkres -config {Clk "/clk_wiz_0/clk_out1 [set PINs]" } [get_bd_pins v_tc_0/clk]
INFO: [tcl 7-1443] No Compatible Board Interface found. Board Tab not created in customize GUI
```

Type a Tcl command here

Vivado 2017.4

File Tools Window Layout View Help Quick Access

Default Layout

Vizle

BLOCK DESIGN - vgaSystem

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design
- PROGRAM AND DEBUG

Diagram

The diagram shows the following components and their connections:

- v_tc_0 (Video Timing Controller)**: Receives `start` and `clk` signals. Its `clk_en` and `gen_clk_en` outputs are connected to `rst_clk_wiz_0_140M`. Its `vsync_out` and `hsync_out[0:0]` outputs are connected to `v_axi4s_vid_out_0`.
- rst_clk_wiz_0_140M (Processor System Reset)**: Receives `slowest_sync_clk` and `clk_wiz_0` signals. Its `mb_reset`, `bus_struct_reset[0:0]`, `peripheral_reset[0:0]`, `interconnect_reset[0:0]`, and `peripheral_resetn[0:0]` outputs are connected to `v_axi4s_vid_out_0`.
- clk_wiz_0 (Clocking Wizard)**: Receives `clk_in1` and outputs `clk_out1`. Its `clk_out1` output is connected to `rst_clk_wiz_0_140M`.
- v_axi4s_vid_out_0 (AXI4-Stream to Video Out)**: Receives `video_in`, `vsync_in`, `ack`, `ack_en`, `rst`, and `vid_in_out_ce` signals. Its `vid_hsync_0` and `vid_vsync_0` outputs are connected to the external bus.

Tcl Console

```

delete_bd_objx [get_bd_nets v_axi4s_vid_out_0_vid_data] [get_bd_ports vid_data_0]

```

Type a Tcl command here

System Net v_axi4s_vid_out_0_vid_ce



<https://vizle.offnote.co>

Contact us: vizle@offnote.co

This document was generated automatically by **Vizle**

Your **Personal Video Reader Assistant**

Learn from Videos **Faster** and **Smarter**

VIZLE PRO / BIZ

- Convert *entire* videos ^{PDF, PPT}
- *Customize* to retain all essential content
- Include Spoken *Transcripts*
- Customer support

Visit <https://vizle.offnote.co/pricing> to learn more

VIZLE FREE PLAN

- Convert videos *partially* ^{PDF only}
- Slides may be *skipped**
- Usage restrictions
- No Customer support

Visit <https://vizle.offnote.co> to try free

Login to Vizle to unlock more slides*