Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the basic operational concepts of the computer with a neat diagram. **(06 Marks)**

b. What is performance measurement? Explain the overall SPEC rating for the computer in a program suite. **(08 Marks)**

c. Explain the following :
(i) Byte addressability (ii) Big-endian assignment (iii) Little-endian assignment. **(06 Marks)**

OR

2 a. Show how the below expression will be executed in one address, two address and three address processors in an accumulator organization.
$X = A \times B + C \times D$ **(08 Marks)**

b. What is the effective address of the source operand in each of the following instructions, when the Register R1, and R2 of computer contain the decimal value 1200 and 4600?
(i) Load 20(R1), R5 (ii) Move #3000, R5 (iii) Store R5, 30(R1, R2)
(iv) Add – (R2), R5 (v) Subtract (R1)+, R5 **(08 Marks)**

c. Interpret the Subroutine Stack Frame with example. **(04 Marks)**

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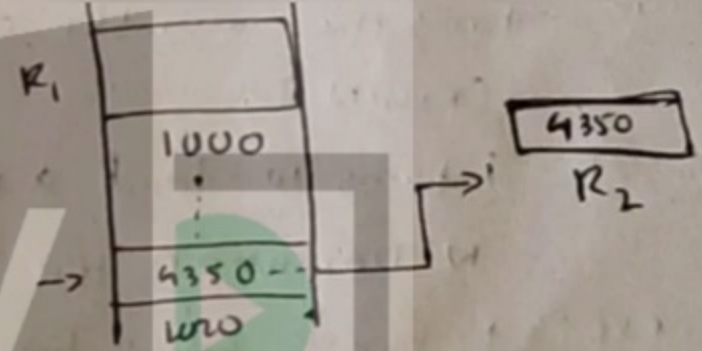
20(R1)

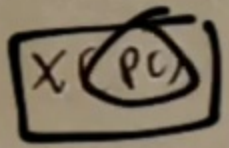
means

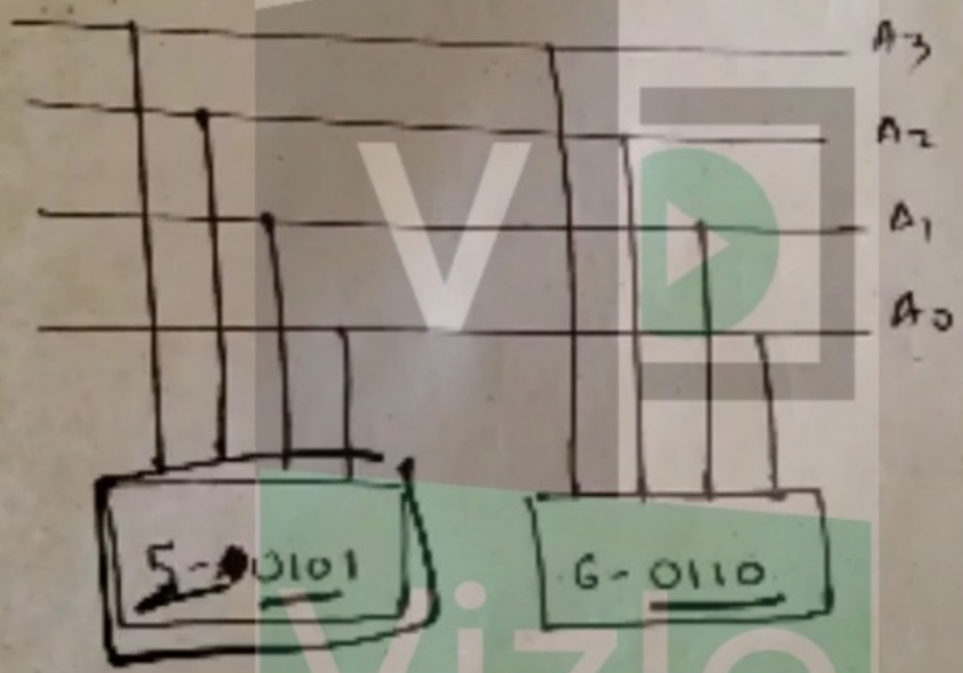
20 locations after R_1



- Relative Addressing

→ Used to point X locations from current location which is in PC.

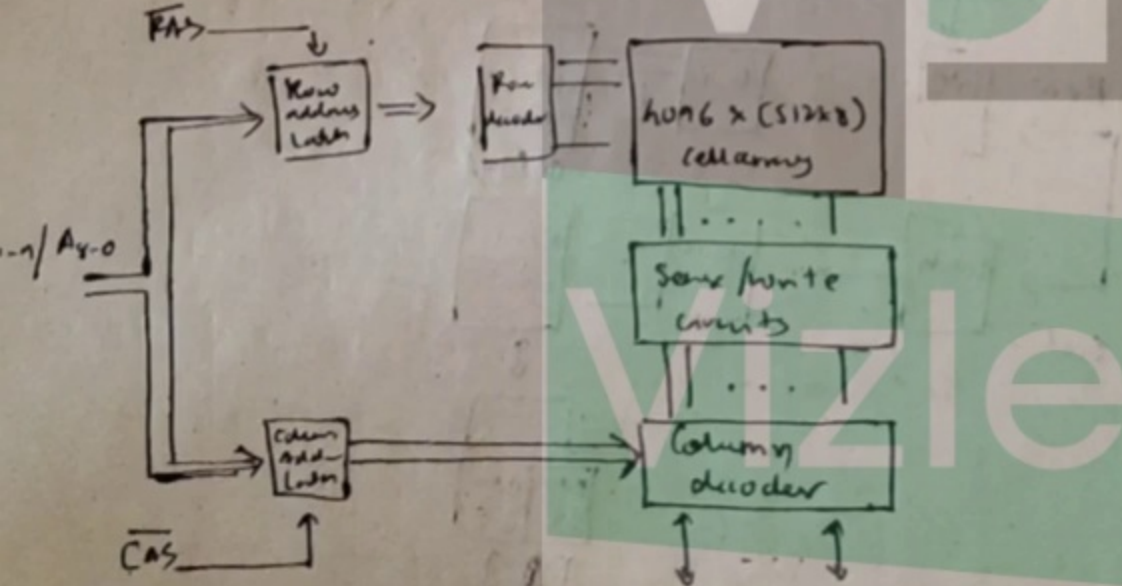



A3
A2
A1
A0
5 - 0101
6 - 0110

Total Rows are 2^{12} = 4096 rows

Total Columns are 2^{9} = 512 columns

Each cell is a byte (8 bits) and for storing the data in each bits, i/p and o/p data lines (8) are required.



M

3

	Register M	Register Q
Initially	0 0 0 1 1	1 0 0 0
Register A	0 0 0 0 0	
Step I: left shift A	0 0 0 0 1 A	0 0 0 □
	+ −M	
Step II: if sign is 0 sub A = A − M	1 1 1 0 1	
	1 1 1 1 0	
Step III: if sign is 1 reset Q_0		0 0 0 0
Step I: left shift A	1 1 1 0 0 A	0 0 0 □

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